

**COLLEGE OF ENGINEERING, CHENGANNUR, KERALA - 689 121.**  
**(Managed by IHRD, A Govt. of Kerala undertaking)**

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No. D<sub>2</sub>/679/18  
01.08.18

Dated :

**SHORT TENDER NOTICE**

Tender No. 01/2018-19, Purchase of FPGA Kits

Last date and time for receipt of : 10.08.18, 2.00 pm  
tender

Date and time for opening of : 10.08.18, 3.00 pm  
tender

Date upto which the rates are to be : 10.09.18  
firm

Price of tender form : Rs. 400/- + ST Rs. 20/-

Price of Duplicate copy : Rs. 200/- + ST Rs. 10/-

Address of Purchasing Officer from : The Principal  
whom tender forms are to be : College of Engineering,  
obtained and to whom tenders are : Chengannur  
to be sent : Kerala 689 121

EMD : 1% of amount quoted

Tender documents can be had from the Principal on payment of the prescribed cost at the counter in cash or by post (postage extra Rs. 35/- for one tender form) sending a DD for the amount payable at Chengannur in favour of the Principal, College of Engineering, Chengannur - 689 121. Details will be available in College website: <http://www.ceconline.edu>

**PRINCIPAL**

SI No	Item with Specification	Qty
1	<p style="text-align: center;"><b>Spartan 6 Trainer Kit</b></p> <ul style="list-style-type: none"> <li>• XC6SLX16 based on Xilinx Spartan -6 FPGA features <ul style="list-style-type: none"> <li>o 14579 Logic cells, 136 Kb of Block Ram</li> <li>o 2 Nos. of Clock Management Tiles (CMT), 2 Nos. of Memory Controller Block (MCB)</li> <li>o 186 User I/O lines, 2278 Kb of distributed RAM</li> <li>o 32 Nos. of DSP Slices</li> </ul> </li> <li>• 16 Nos. of digital input using slide switches with LED indication</li> <li>• 16 Nos. of digital output using discrete LEDs</li> <li>• 16x2 LCD is provided for display the text message</li> <li>• One reset switch</li> <li>• One switch for giving manual clock</li> <li>• FPGA configuration through</li> <li>• On Board Xilinx USB to JTAG Programmer with isolation to configure FPGA <ul style="list-style-type: none"> <li>o On Board Flash Prom XCF04S (Programmable through USB to JTAG Programmer)</li> </ul> </li> <li>• Total 186 I/O Pins: 100 Pins used for integrating peripheral like LED, Switches etc., balance pins are available to user in 3 Nos. of 20 pin header.</li> <li>• 1 No of 26 pin header to interface VLIM cards like Traffic Light Controller / On-board TLC factory settable.</li> <li>• On board programmable PLL oscillator from 1 MHz to 100 Mhz using jumpers</li> <li>• 4 Nos. of 7 segment LED display</li> <li>• One relay and Buzzer provided</li> <li>• Stepper &amp; DC motor drive provided on board (Motor Optional)</li> <li>• 4 x 4 matrix key provided</li> <li>• On Board 1<sup>2</sup>C RTC interface</li> <li>• On Board Temperature sensor interface</li> <li>• SPI based Analog to Digital Converter <ul style="list-style-type: none"> <li>o Resolution : 12 bits</li> <li>o Number of Channel : 2 Channel</li> <li>o Input Range : 0 to 3.3 V</li> <li>o Speed : 1 Msps</li> </ul> </li> <li>• SPI Based Digital to Analog Converter <ul style="list-style-type: none"> <li>o Resolution : 12 bits</li> <li>o Number of Channel : 2 Channel</li> <li>o Input Range : 0 to 3.3 V</li> <li>o Speed : 8.5 μS setting time</li> </ul> </li> <li>• ADC Inputs and DAC outputs are terminated at J801 connector</li> <li>• Housed in a sleek plastic cabinet with built in SMPS 5V/2A</li> <li>• Compatible with Xilinx ISE Web PACK Software (Version 12.1 and above)</li> </ul>	10 Nos.

1. Rate: Should be inclusive of all taxes and duties.
2. Delivery should be made at site College of Engineering, Chengannur
3. Warranty :- 1 year with after sales support

4. Payment : 100% after successful testing
5. Security Deposit : 5% of the contract amount

**PRINCIPAL**